Experimental validation of the surface state distribution model in the Suzuki theory to qualify the thin film surface materials

Laurent Pichon, K. Yang, Anne-Claire Salaün

Experimental validation of the surface state distribution model in the Suzuki theory to qualify the thin film surface materials

L. Pichon*, K. Yang, A-C.Salaün

Institut d'Electronique et des Télécommunications de Rennes, UMR CNRS 6164, Université de Rennes 1, campus de beaulieu, 263 avenue du général Leclerc, 35042 Rennes cedex, France, phone: +33223235665, fax: +33223235657, *laurent.pichon@univ-rennes1.fr

*Corresponding author: lpichon@univ-rennes1.fr

Keywords: Suzuki theory, surface state density, field effect conductance, polycrystalline silicon, thin film transistors

The relevance of the theoretical Suzuki's model of surface state density to determine the surface states distribution at the active layer/silicon dioxide interfaces is carried out in polycrystalline silicon thin film transistors (TFTs) issued from two different crystallization technologies of the active layer: furnace solid phase crystallized (FSPC) and laser solid phase crystallized (LSPC) TFTs. The experimental validation of this model is demonstrated using the field effect conductance method. Results show that distribution is higher for the FSPC TFTs in relationship with the process crystallization of the active layer. In addition, it is shown that theoretical surface state model allows discriminating dangling bonds states and tail states distributions and acts as relevant model to qualify the surface of thin film material.

I. INTRODUCTION

Since the earlier of the 90s, applications based on electronic components manufactured from thin-film semiconductors is widely spread, in particular for visualization systems [1,2], and more recently for electronics systems on flexible substrates [3-5]. These semiconductors have poorer properties than those of bulk materials, because of their disordered structure, or because of the appearance of defects induced by their specific uses (mechanical stress…) [6]. The performances of the corresponding applications are strongly related to the thin film transistor (TFT), basic active component constituting the electronic of the system. The development of TFTs based electronics requires relevant diagnostic tools to assess electronic properties of the systems, both strongly related to the active layer/gate insulator interface and active layer qualities of the transistor. In this way, several methods of electrical characterization to qualify TFT manufacturing technologies were developed, in particular for the widely used silicon thin film technology still acting as reference.

Electrical behaviour of thin film silicon layer is different from single bulk silicon due to higher defect density originating from polycrystalline structure. In this case, the electronic transport is strongly affected by the carriers trapping effects of these defects [7]. Two main causes of defects are usually invoked: dangling bonds and strained bonds corresponding to deep and shallow level trap states distributed into the band gap respectively. Two types of numerical models for state distributions are then considered: Gaussian distribution with a maximum around midgap and exponential band tailing corresponding to dangling bonds and strained bonds type defects respectively [8-10]. The corresponding states energy distributions are representative of the crystal quality of the material. In this way, many studies have been devoted to the determination of the density of states (DOS) into the layer and surface state density (N_{SS}) energy distributions used as diagnostic tools. Methods based on capacitance, resistivity, conductance activation energy and low frequency noise measurements exist to determine these distributions [9] [11-13]. However, few methods allow the discrimination of the deep level state energy distribution from the high level one

as hyperfine diagnostic tools. Characterization of polycrystalline silicon (poly-Si) and active layer/SiO_2 interface qualities are fundamental for the well understanding of electrical properties of poly-Si thin film based MOS devices.

In this study, active layer/SiO_2 interface quality in poly-Si thin film transistors is characterized by the determination of the densities of defect states into the bandgap using Suzuki's theory model [14]. This theory reports on two models for the determination of the density of states distribution for defects located into the active layer (DOS) and at the interface (N_{SS}) respectively. In this theory DOS and N_{SS} calculations are based on the surface potential dependence with the gate voltage and on the conductance of the TFT. DOS is classically and commonly determined following Suzuki's theory, and thus refers to the active layer morphology and crystal quality (*ie* defects responsible of carriers trapping) [15]. However, to our knowledge N_{SS} experimental determination has never been conducted following Suzuki's theory, because in this case the surface potential with gate voltage dependence specifically requires C-V characteristics. Indeed, C-V measurements are difficult to implement for polycrystalline silicon TFTs, especially because of the high defect density into the insulator and at the insulator/active layer interface. To overcome this drawback, temperature measurements of the field effect conductance has been firstly used as alternative approach for N_{SS} determination according Suzuki model. Following this method, our analysis reports on the first experimental validation of the determination of the state distribution at the surface of the poly-Si thin films based on Suzuki's theoretical surface states model, and discrimination of the nature of involved defects is originally shown using this model.

II. EXPERIMENTAL DETAILS

TFTs used in this study are fabricated by a low temperature (≤ 600°C) four masks process, and are fabricated on glass substrate covered with a SiO_2 layer. Active layer is made of non-intentionally doped amorphous silicon (as-Si) deposited by LPCVD (low chemical vapor pressure deposition). Gate insulator is made of silicon dioxide layer deposited by CVD process at atmospheric pressure. Source/Drain regions are built in LPCVD highly *in-situ* doped as-Si layer using phosphine gas. Source and drain electrodes are made of thermally evaporated aluminium. Active layer thickness is 150nm, gate insulator is 100nm and 70nm thick for FSPC and LSPC TFTs respectively.

TFTs are issued from two different crystallization techniques of the active layer: Furnace Solid Phase Crystallized (FSPC) poly-Si TFTs and Laser Solid Phase Crystallized (LSPC) poly-Si TFTs. For FSPC TFTs, a thermal annealing in nitrogen ambient ensures crystallization of the as-Si active layer, and for LSPC TFTs an additional SPC thermal annealing of the active layer is carried out by an Argon laser beam. In addition, for FSPC TFTs channel, Source/Drain are built in one amorphous silicon layer with two differently doped stack regions (the lower part stating as active layer is undoped, and the upper part is highly doped as source /drain regions). For LPC TFTs two amorphous silicon layers are deposited (a undoped one as active layer and a second one highly doped as source/drain regions). More details about the fabrication process of the TFTs are reported in the ref [13].

The static I-V electrical characteristics of the devices are collected at room temperature using an Agilent B1500A semiconductor parameter analyser. Temperature measurements were carried out from 300 to 400K using a temperature controlled wafer probe system [16].

Figure 1 shows transfer characteristics plotted in semilog scale for FSPC and LSPC TFTs operating the in linear mode, representative of more than ten of each type of tested devices. The

LSPC TFTs exhibits better electrical performances. The on-state current is higher, the threshold voltage (V_{TH}) is lower and the switching properties (subtrhreshold slope S) are better: V_{TH} = 6.3V and

S = 1.4V/dec for FSPC TFTs, V_{TH} = 2.4V and S = 0.4V/dec for LSPC TFTs. In addition, one can remark that no significant gate voltage shift of the transfer characteristics is observed, and that improvement of the electrical properties in LSPC TFTs is mainly related to the subthreshold slope due to improvement of the interface quality.

III. MODEL OF INTERFACE STATE DISTRIBUTION

There are two main complementary approaches based on analytical methods [12,14] or temperature measurements of the current [8] previously established to qualify active layer by determination of the DOS and the N_{SS} in amorphous or polycrystalline silicon TFTs. These methods are based on the analysis of the field-effect conductance, and it has been usually admitted that it is sensitive enough to account for the effect of the silicon film morphology.

Following Suzuki's theory [14], the calculations are mainly focused on the distribution of states density into the active layer [15, 17], but the determination of surface state density in relation to surface quality of material has never been experimentally studied. However, the induced surface charge density, Q_{SS}, at localized interface traps is given by [14]:

$$Q_{SS}(\psi_s) = d\psi_s \frac{G_0}{dG}\frac{\varepsilon_{si}}{d_{si}}\left[\exp\frac{q\psi_s}{kT} - 1\right] - \frac{\varepsilon_{OX}}{d_{OX}}(V_{GS} - V_{FB} - \psi_s) \quad (1)$$

where Ψ_S refers to the potential at the SiO_2/Si interface, G_0 is the conductance at the flatband voltage (i.e. Ψ_S=0), ε_{Si} the dielectric constant of the silicon, ε_{OX} the dielectric constant of the oxide,

d_{OX} the thickness of the gate oxide, d_{Si} the active layer thickness, V_{FB} the flatband voltage, V_{GS} the gate bias, k the Boltzman constant, T the temperature and q the elementary electrical charge.

The induced charge trapped at the interface is given by:

$$Q_{SS}(\psi_s) = -q\int_{E_{F0}}^{E_{F0}+q\psi_s} N_{SS}(E)\,dE \qquad (2)$$

where N_{SS} stands for the energy distribution of surface state density, $E_{F0} = E_{C(bulk)} - E_F$, with E_F the equilibrium fermi level position and $E_{C(Bulk)}$ the conduction band energy. Therefore, the surface state density is deduced from [14]:

$$N_{SS}(E_{F0} + q\psi_s) \cong -\frac{1}{q}\frac{\partial Q_{SS}(\psi_s)}{\partial(q\psi_s)} \qquad (3)$$

A calculation of Q_{SS} given by (1) is firstly needed for the determination of N_{SS}. This approach is based on the use of the experimental variations of the conductance G with the gate voltage V_{GS}, and the knowledge of the dependence of the surface potential Ψ_S with V_{GS}. Two approaches have been previously developed. In the first one [14], iterative process with $\Psi_S(i) = \Psi_S(i-1) + d\Psi_S$ is used to numerically approximate the relation $\Psi_S = f(V_{GS})$. In this case the increment of Ψs can be theoretically determined from C-V characteristics, but difficult to plot for polycristalline silicon based MOS capacitor. In the second method [8], the experimental measurements of the drain current with temperature are exploited: the deduced activation energy, E_a, makes it possible to state Ψ_S dependence on V_{GS} following (see fig. 2):

$$q\psi_s \cong E_{F0} - E_a(V_{GS}) \qquad (4)$$

with E_{F0} the activation energy for $V_{GS} = V_{FB}$ (corresponding to the minimum of the drain current of the transfer characteristics).

In this study, calculation of N_{SS} has been carried out following $qd\psi_s \approx -\left(\frac{\partial E_a}{\partial V_{GS}}\right) dV_{GS}$ deduced from the $E_a = f(V_{GS})$ curves for the FSPC and LSPC TFTs plotted in the figure 3, with dV_{GS} = 50mV. Variation of the conductance is obtained by $dG = dV_{GS}(g_m/V_{DS})$ for TFTs operating in the linear mode.

According to (1) negative values, due to electrons trapping at defects, were admitted for calculations of Q_{SS}. In this study flatband voltage is determined as the voltage where the drain current is the minimum, and then calculations were carried out with V_{FB} = - 4V (E_{F0} = 0.48 eV) and V_{FB} = - 3V (E_{F0} = 0.52 eV) for the FSPC and LSPC TFTs respectively. Activation energy was determined from the slope of the linear Arrhenius plots Ea = f(1/T).

IV. RESULTS AND DISCUSSION

The plots of the calculated N_{SS} for the two types of TFTs are reported in the figure 4. Values are consistent with previous results obtained by other methods [12,13]. In addition, the results show that surface states distribution is lower for the LSPC TFTs, more particularly in the lower part of the bandgap. This tendency is also observed for the DOS calculated by the Suzuki's incremental method in the core of the poly-Si active layer (fig. 4. (b)) and confirm that. These results agree with the decrease of the electrical performances (higher threshold voltage and subthreshold slope, lower On-state current) of the FSPC transistor (see fig. 1). This means that the active layer/SiO_2 interface and poly-Si active layer qualities are better thanks to the beneficial effect of the additional laser annealing. Indeed, laser annealing has been commonly used to improve the electrical properties of

TFTs due to a decrease of the defect density into the poly-Si active layer [18-20]. Moreover, it is noted that the contribution shape of state distribution for the deep states (*ie* the increase of density when energy level decreases) is more noticeable for LSPC TFT and refers to theoretical Gaussian-type distribution to model defects, because of evident presence of dangling bonds (acting as acceptor like states in our case) at the interface between two materials. These observations agree with a previous work [13] reporting on the determination by low frequency (1/f) noise measurements of interface state distribution in these polycrystalline silicon TFTs. In this study, noise analysis has been supported by the theory of charge carrier trapping/detrapping due to defects located at the interface.

Both interface and bulk states distributions are mainly related to the spatial distribution of defects either located at the surface and/or in the core of the polycrystalline silicon layer in relation to the crystallization process. Indeed, crystallization of a-Si layer starts at the seed nucleation layer located in the SiO_2/a-Si layer bottom interface. In this case, grains growth vertically in a columnar type structure, resulting to higher defects density (including grain boundaries) at the surface of polycrystalline silicon active layer (see fig. 5). This grain morphology and structural defects density were previously revealed by scanning electron microscopy study [21].

Based on the results of a previous numerical study [12], the deep state distribution could be related to defects mainly located at grain boundaries of the poly-Si layer located at the active layer/SiO_2 gate insulator interface. These grain boundaries, usually recognized as places for dangling bonds, act as traps areas and strongly affect the field effect conductance of the transistors [7]. Therefore, according to the plots reported in the fig. 4 the SPC laser annealing induces a significant lowering of the strained bonds type defects density close to the interface. However, the reduction is not so significant for LSPC TFT. Two reasons could be invoked to explain it. The first one is because solid phase laser annealing does not present a high degree of crystal quality as usually provided by others laser liquid crystallization process. In this case, crystallization from

liquid to solid phase results to higher crystal quality of the polycrystalline silicon active layer with higher grain size and lower intra-grain defects after re-solidification, leading to better electrical performances of the TFTs [18-20, 22, 23]. The second possible explanation is because at high gate voltages (*ie* in the strong inversion) conductance of the transistor is rather controlled by access resistance related to the active layer/Drain (Source) region interfaces, and thus responsible of a higher defect density at shallow energy level observed in LSPC TFTs. On other hand, for devices operating from the depleted to inversion mode (*ie* in the switching region) the conductance is strongly affected by the trapping effects of carriers (at grain boundaries) into the channel region. This means that the state distribution determination is relevant in the lower part of the bandgap.

These distributions deduced from the theoretical Suzuki's surface model highlight the separated contributions of the type of defects (see fig. 2). Such distribution behavior related to the deep state defects for the DOS was not observed in previous work [24], and neither for our studied TFT (fig. 4. (b)). This means that model of calculation of DOS into the bandgap classically used by Suzuki method is an incomplete view of defects distribution at the surface and into the core of the active layer. Therefore, our results demonstrate that surface states model of Suzuki is a relevant and complementary diagnostic tool for surface characterization of thin film material.

V. CONCLUSION

Capacitance voltage measurements on MOS (or MIS) devices are commonly used to qualify surface crystalline materials. However, this method is not convenient for disordered materials because of high defects density at insulator/material interface. In this study, surface quality of polycrystalline silicon thin films is investigated, based on the surface state theoretical model of Suzuki, and using temperature measurements of field effect conductance. Results show a higher surface state density for FSPC polycrystalline silicon TFTs. This is explained because the active

layer of FSPC TFT do not have the same specifications in terms of morphology and crystal quality because of the crystallization thermal annealing.

Transistors characteristics combined with analysis of energy distribution of defects density based on the Suzuki's surface states model is another way to fully characterize surface of poly-Si layers in relation to its morphology. This method proposed in this study allows discrimination of the nature of surface defects involved in trapping of carriers, and can be extendedly used as hyperfine diagnostic tool in complement of the usual determination of DOS, for surface characterization of non crystalline thin layers.

References

[1] Someya S et al. TFT active matrix liquid crystal display devices 1992; US patent N° 5132820

[2] Stewart M et al. Polysilicon TFT Technology for Active Matrix OLED Displays. IEEE Trans on Elec Dev. 2001; 48(5): 845

[3] Chen Y et al. Flexible active-matrix electronic ink display. Nature Com. 2003; 423, 136

[4] Inoue S et al. Surface-free technology by laser annealing (SUFTLA) and its application to poly-Si TFT-LCDs on plastic film with integrated drivers. IEEE Trans Elect Dev 2002; 49(8), 1353-1360

[5] Kim J et al. Stretchable silicon nanoribbon electronics for skin prosthesis, Nature Comm. 2014; 5:5747

[6] Lee M H et al. Electrical properties correlated with redistributed deep states in a-Si:H thin film transistors on flexible substrates undergoing mechanical bending. Thin Sol Films. 2013; 528, 82-85

[7] J. W. Seto. The electrical properties of polycristalline silicon films. Journ Appl Phys 1975: 46, 5247

[8] Fortunato G et al. Field-effect analysis for the determination of gap-state density and Fermi level temperature dependence in polycristalline silicon. PhiL Mag 1988; B, **57**, 573

[9] Hirae S et al. Energy distribution of trapping states in polycristalline silicon. Journ Appl Phys 1980; **51**, 1043

[10] Pesic I et al. Degradation of 4H-SiC IGBT threshold characteristics due to SiC/SiO2 interface defects. Sol Stat Elect 2014; **101**, 126

[11] Yamamoto Y et al. Energy distribution of trapping states at grain boundaries in polycristalline silicon Journ Appl Phys 1992; **71**, 3350

[12] Dimitriadis C A et al. Determination of bulk states and interface states distributions in polycristalline silicon thin-film transistors Journ Appl Phys 1993; **74**, 2919

[13] Pichon L et al. Improvement in the determination by 1/f noise measurements of the interface state distribution in polysilicon thin film transistors in relation with the compensation law of Meyer Neldel. Journ Appl Phys 2009; **105**, 104503

[14] Suzuki T et al. Theoretical interpretations of the gap state density determined from the field effect and capacitance-voltage characteristics of amorphous semiconductors Jap Journ Appl Phys.1982; **21**(3), L159

[15] M. H. Lee M H et al. Correlation between gap state density and bias stress reliability of nanocrystalline TFTs comparing with hydrogenated amorphous silicon TFTs. Sol St Elec. 2013; **80**, 72-75

[16] Cordier C et al. « Low frequency noise model in N-MOS transistors operating from sub-threshold to above regions » Sol St Elect. 2005; 49, pp 1376-1380

[17] Fortunato G and Migliorato P. Determination of gap state density in polycristalline silicon by field-effect conductance. Appl Phys Lett. 1986; **49**(16), 1025

[18] Sera K et al. High-Performance TFT's Fabricated by XeCl Excimer Laser Annealing of Hydrogenated Amorphous-Silicon Film. IEEE Trans on Elect Dev. 1989; 36(12), 2868-2872

[19] Khono A et al. High performance poly-Si TFTs fabricated using pulsed laser annealing and remote plasma CVD with low temperature processing. IEEE trans Elect Dev. 1995; 42(2), 251-257

[20] Angelis C T and Dimitriadis C A. Effect of excimer laser annealing on the structural and electrical properties of polycrystalline silicon thin-film transistors. Journ Appl Phys. 1999; 86, 4600

[21] Haji L et al. Mode of growth and microstructure of polycristalline silicon obtained by solid-phase crystallization of an amorphous silicon film Journ Appl Phys. 1994; **75**(8), 3944

[22] L. Mariucci et al. Crystallization mechanisms in laser irradiated thin amorphous silicon films Thin Solid Films 2003; **427**, 91

[23] F.Plais, P.Legagneux et al. Low temperature polysilicon TFTs: a comparison of solid phase and laser crystallization Micrelect. Eng. (1995); **28**, 443

[24] Le Borgne B et al. Electrical properties of self-aligned gate-all-around polycristalline silicon nanowires field-effect transistors Microelec Eng. 2016; **150**, 32

FIGURE CAPTIONS

Figure 1: Transfer characteristics of FSPC and LSPC TFTs at V_{DS} = 1V (linear mode).

Figure 2: Energy band diagram of a metal/oxide/semiconductor (MOS) structure with a positive gate voltage (in accumulation mode), and surface states density (N_{SS}) resulting from gaussian (dangling bonds) and exponential (strained bonds) state distributions

Figure 3: Plots of the activation energy versus the gate voltage for FSPC and LSPC TFTs.

Figure 4: Active layer/silicon dioxide interface states distribution calculated for FSPC and LSPC TFTs (a) and plots of the corresponding DOS (b)

Figure 5: Schematic cross section views illustrating the columnar type structure of a polycrystalline silicon layer.

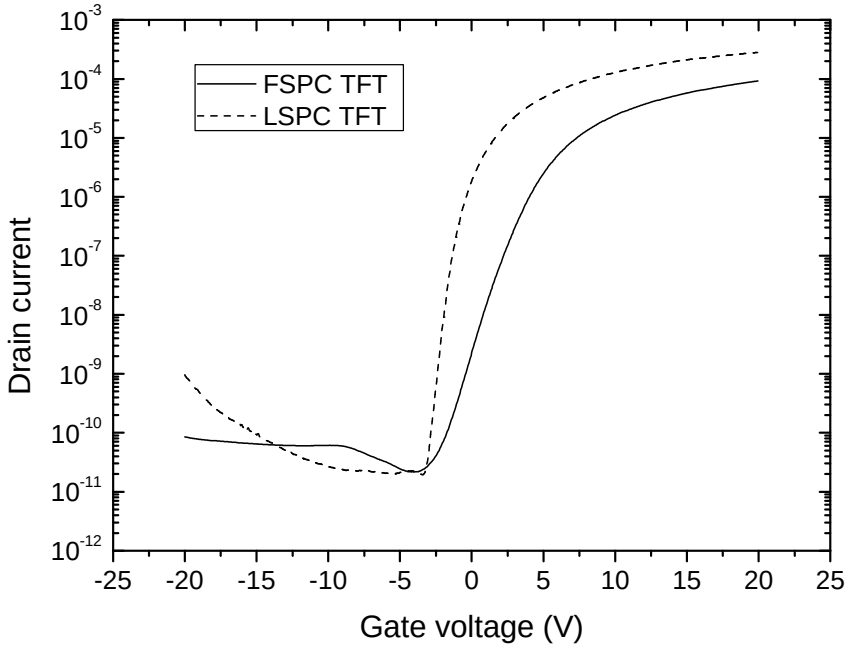

FSPC TFT
LSPC TFT
Drain current
Gate voltage (V)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
-25
-20
-15
-10
-5
0
5
10
15
20
25

Figure 1

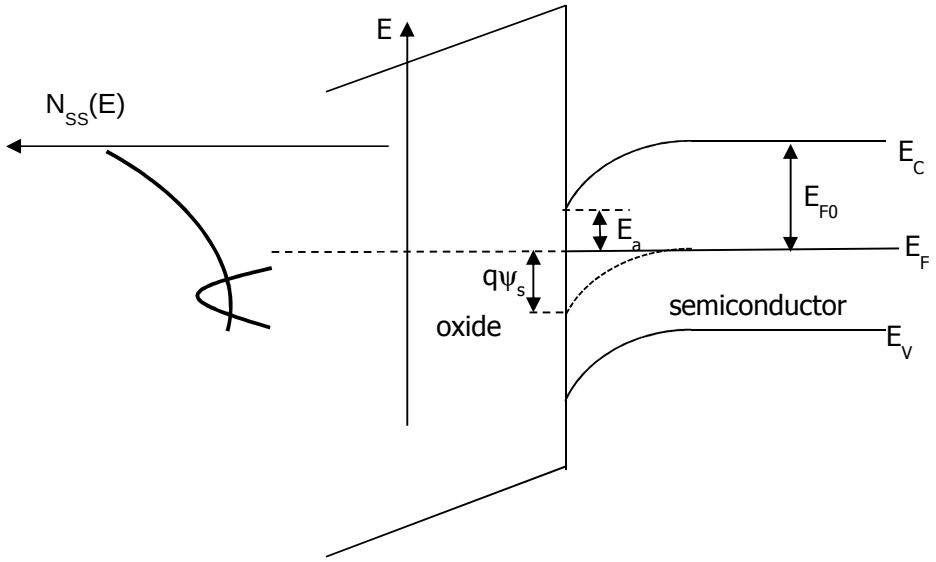


Figure 2

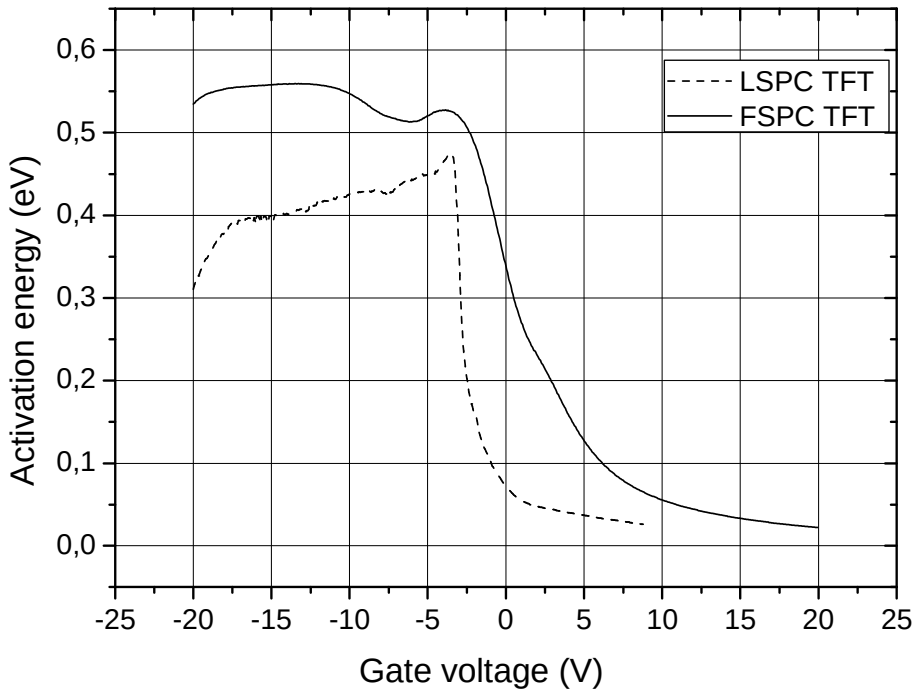
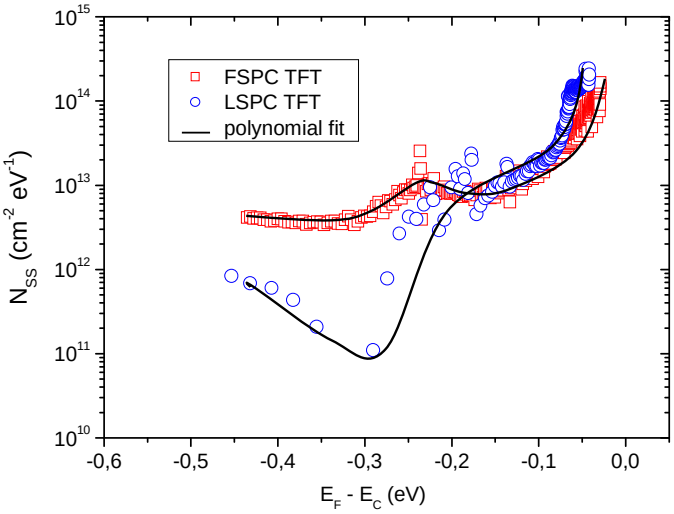
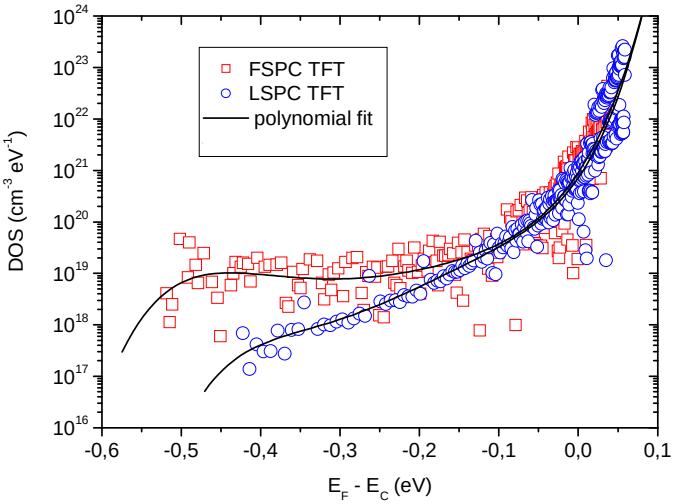

LSPC TFT
FSPC TFT
Activation energy (eV)
Gate voltage (V)
0,0
0,1
0,2
0,3
0,4
0,5
0,6
-25
-20
-15
-10
-5
0
5
10
15
20
25

Figure 3


FSPC TFT
LSPC TFT
polynomial fit
N_{SS} (cm^{-2} eV^{-1})
E_F - E_C (eV)

(a)


FSPC TFT
LSPC TFT
polynomial fit
DOS (cm^{-3} eV^{-1})
E_F - E_C (eV)

(b)

Figure 4

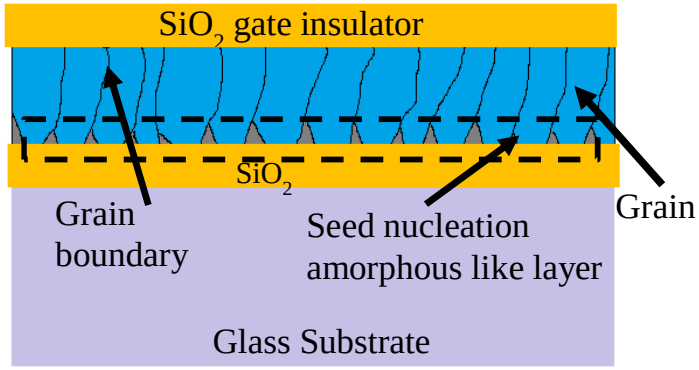

SiO2 gate insulator
SiO2
Grain
boundary
Seed nucleation
amorphous like layer
Grain
Glass Substrate

Figure 5